Sheet: cpu
File: cpu.sch

Sheet: timing
File: timing.sch

Sheet: addrmux
File: addrmux.sch

Sheet: memory
File: memory.sch

Sheet: power
File: power.sch

Sheet: input
File: input.sch

Sheet: ldp
File: ldp.sch

Sheet: misc
File: misc.sch

Sheet: video
File: video.sch

This is the edge connector of the PCB.
Caution: It is backwards from Interstellar (ie upside down).

CN100
Esh_Edge

GND	1	A	GND
	2	B	
VCC	3	C	VCC
	4	D	
	5	E	
LAMP_START2	6	F	LAMP_START1
LAMP_JOYSTICK	7	H	LAMP_ACTION
SWITCH_UNK2	8	J	SWITCH_UNK1
SWITCH_DOWN	9	K	SWITCH_UP
SWITCH_LEFT	10	L	SWITCH_RIGHT
SWITCH_ACTION2	11	M	SWITCH_ACTION
SWITCH_TEST	12	N	SWITCH_UNK3
SWITCH_START1	13	P	SWITCH_COIN1
SWITCH_COIN2	14	R	GND
SWITCH_START2	15	S	
ANALOG_RED	16	T	ANALOG_GREEN
ANALOG_BLUE	17	U	CSYNC_OUT
SHOW_LD_VIDEO	18	V	DISC_CSYNC
DISC_VSYNC	19	W	
12V	20	X	12V
	21	Y	
GND	22	Z	GND

These connectors are optional.
I included them to make it easier to verify accuracy of the PCB clone.
These connectors were likely used in order to test the game without using the edge connector.

CN6
Conn_02x13_Counter_Clockwise

	1	26	
	2	25	
	3	24	
	4	23	
	5	22	
	6	21	
ANALOG_GREEN	7	20	
CSYNC_OUT	8	19	
DISC_CSYNC	9	18	
DISC_VSYNC	10	17	
SHOW_LD_VIDEO	11	16	
ANALOG_BLUE	12	15	
ANALOG_RED	13	14	

GND

CN2
Conn_02x13_Counter_Clockwise

RA2_P7	1	26	RA3_P3
GND	2	25	RA3_P8
RA2_P4	3	24	RA1_P5
	4	23	RA1_P9
SWITCH_START1	5	22	SWITCH_START2
	6	21	SWITCH_TEST
D2_P16	7	20	LAMP_START1
D2_P15	8	19	LAMP_START2
SWITCH_RIGHT	9	18	SWITCH_LEFT
LAMP_ACTION	10	17	SWITCH_UP
SWITCH_DOWN	11	16	SWITCH_ACTION
LAMP_JOYSTICK	12	15	SWITCH_ACTION2
SWITCH_COIN2	13	14	SWITCH_COIN1

HOLE1 MountingHole
HOLE2 MountingHole
HOLE3 MountingHole
HOLE4 MountingHole
HOLE5 MountingHole
HOLE6 MountingHole

These power flags are needed so KiCad knows that power is coming from outside of this PCB.

PWR_FLAG (RAM_PWR)
PWR_FLAG (GND)
PWR_FLAG (VCC)

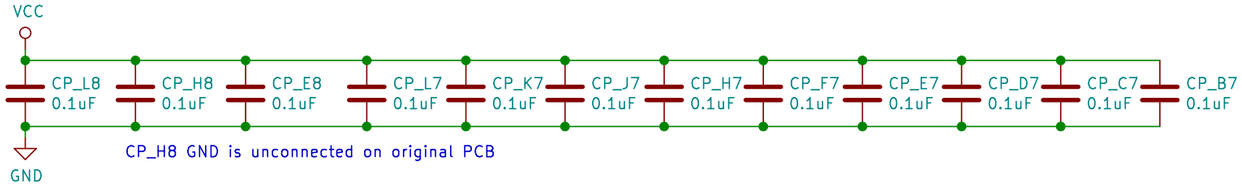
Original PCB supplied by Antonio Nati
Reverse engineered by Matt Ownby with help from Warren Ondras
RuleCity LLC

Sheet: /
File: esh.sch

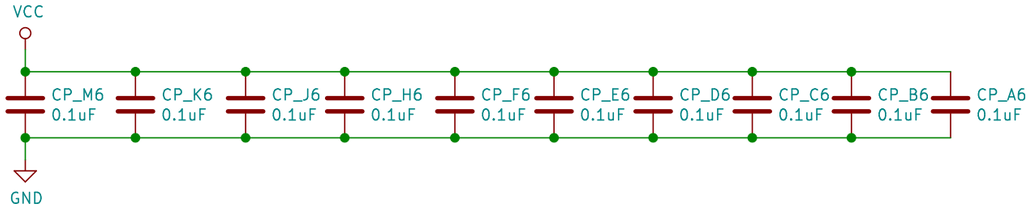
Title: Esh's Aurunmilla

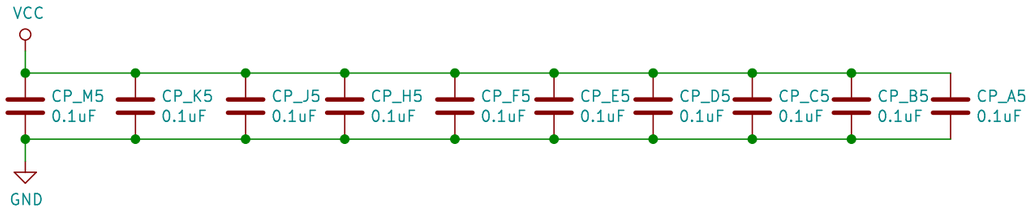
Size: A3	Date: 2021-03-22	**Rev: 3**
KiCad E.D.A. kicad (5.1.5)-3		Id: 1/10

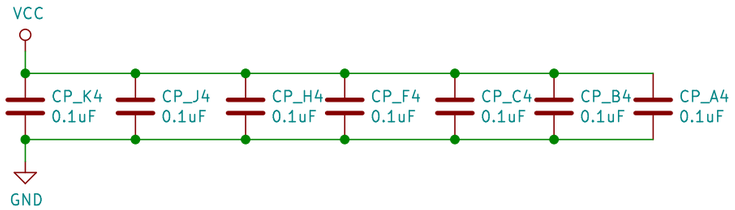
If capacitor doesn't line up with a letter on PCB, take the letter that is below the capacitor.

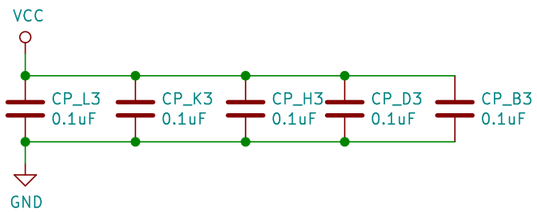


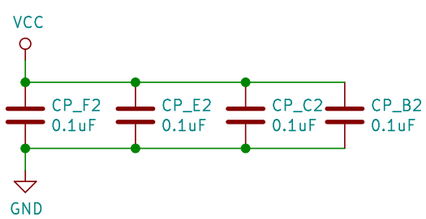
CP_H8 GND is unconnected on original PCB



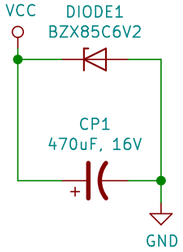


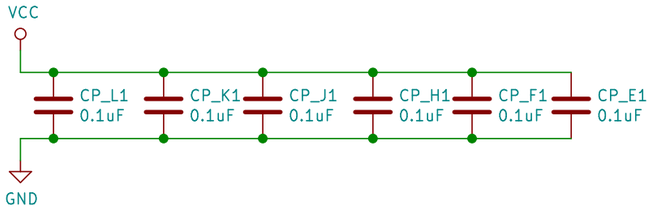






This diode sacrifices its life if the edge connector is installed upside down.
If not too much current is applied, the rest of the PCB may be saved if this happens.





Original PCB supplied by Antonio Nati
Reverse engineered by Matt Ownby with help from Warren Ondras
RuleCity LLC

Sheet: /power/
File: power.sch

Title: Esh's Aurunmilla

Size: A4	Date: 2021-03-22	**Rev: 3**
KiCad E.D.A. kicad (5.1.5)-3		Id: 2/10

VA0 VA1 VA2 VA3 VA4 VA5 VA6 VA7

RST_V_CNTRS CLK_7_8kHz CLK_18_432MHz DSC_CSYNC_BEGIN DSC_VSYNC_BEGIN CHD3 CHD2 CLK_6_144MHz

HA0 HA1 HA2 HA3 HA4 HA5 HA6 HA7

CVD0 CVD1 CVD2 CHD0 CHD1 CHD2 CHD3

CLK_15_6kHz HIDE_LD_VIDEO CLK_15_6kHz CSYNC_OUT

Having D5 pin 3 unconnected is a defect on the original PCB, kept here for documentation purposes.
The game works despite the defect.
The proper fix is to tie this pin to VCC.

D7 74LS161
about 244 Hz
about 122 Hz
59.5 Hz
59.5 Hz (oddly enough)

D6A 74LS107
D6B 74LS107

D5A 74LS139
D5_P4 Always high on real Esh PCB
D5_P6 60 Hz on real Esh PCB

D5B 74LS139

RA10 1k

C7 74LS161
about 4 kHz
about 2 kHz
about 1 kHz
about 500 Hz

C6 MB7052
C5 MB7052
C4 74LS273

NOTE: Estimated timing is assuming PCB edge connector is unplugged except for 5V/GND. This ensures that vsync/csync is being generated by PCB and not coming from the superimpose PCB.

X1 18.432 MHz
R21 330
CP28 100pF
R20 330
B7 74LS368

B6 74LS161
B5 74LS161
B4 74LS161
B3 74LS161
about 187.6 kHz
about 93.8 kHz
about 46.9 kHz
about 31.25 kHz
3.072 MHz
1.536 MHz
768 kHz
384 kHz

CP28 may need to be adjusted depending on your crystal.

A6A 74LS30
A5A 74LS08
A5B 74LS08
A4A 74LS86
A4B 74LS86
A4D 74LS86
A5C 74LS08
A5D 74LS08
A4C 74LS86
R18 100
R17 1k
This is CSYNC

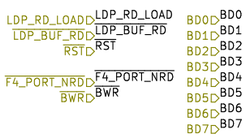
A6B 74LS30
A5E 74LS08
A4E 74LS86
D6C 74LS107
D5C 74LS139

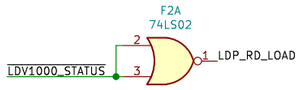
Original PCB supplied by Antonio Nati
Reverse engineered by Matt Ownby with help from Warren Ondras
RuleCity LLC

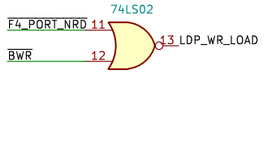
Sheet: /timing/
File: timing.sch

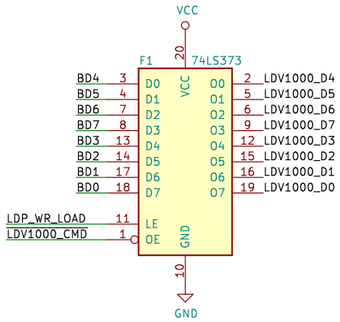
Title: Esh's Aurunmilla

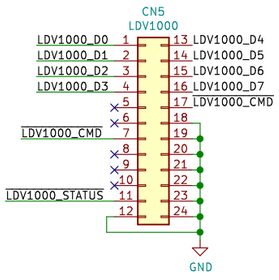
Size: A3	Date: 2021-03-22	**Rev: 3**
KiCad E.D.A. kicad (5.1.5)-3		Id: 3/10

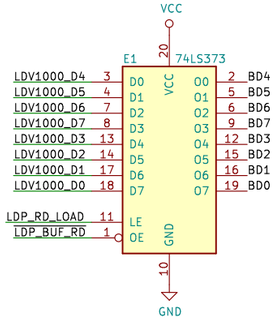


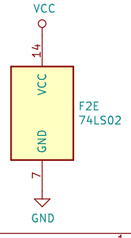












Original PCB supplied by Antonio Nati
Reverse engineered by Matt Ownby with help from Warren Ondras
RuleCity LLC

Sheet: /ldp/
File: ldp.sch

Title: Esh's Aurunmilla

Size: A3	Date: 2021-03-22	**Rev: 3**
KiCad E.D.A. kicad (5.1.5)-3		Id: 4/10

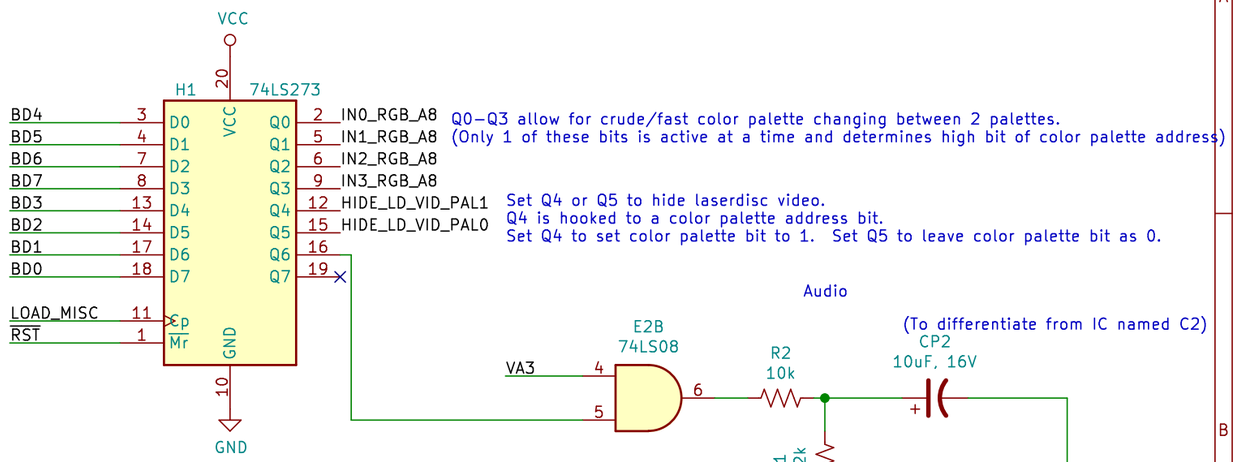
BA0
BA1
BA2
F8-FF_PORT_WR
LOAD_MISC
RST
CLR_NMI
CLR_INT
VA3

IN0_RGB_A8
IN1_RGB_A8
IN2_RGB_A8
IN3_RGB_A8
HIDE_LD_VID_PAL1
HIDE_LD_VID_PAL0

BD0
BD1
BD2
BD3
BD4
BD5
BD6
BD7

LAMP_START2
LAMP_START1
LAMP_JOYSTICK
LAMP_ACTION
12V
D2_P15
D2_P16

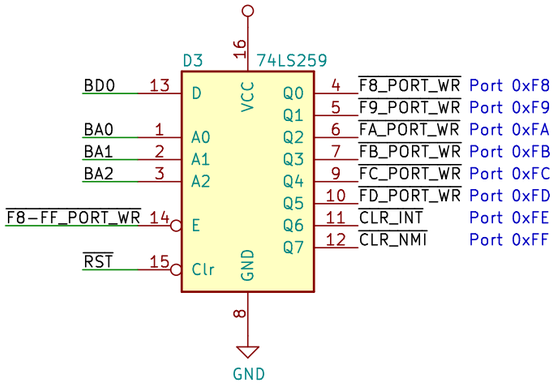
This gets set when port F5 is written.

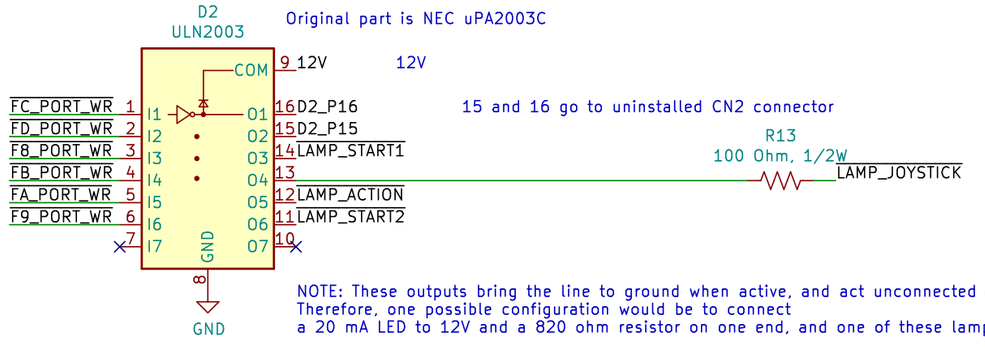


Q0–Q3 allow for crude/fast color palette changing between 2 palettes.
(Only 1 of these bits is active at a time and determines high bit of color palette address)

Set Q4 or Q5 to hide laserdisc video.
Q4 is hooked to a color palette address bit.
Set Q4 to set color palette bit to 1. Set Q5 to leave color palette bit as 0.

Audio





NOTE: These outputs bring the line to ground when active, and act unconnected otherwise.
Therefore, one possible configuration would be to connect
a 20 mA LED to 12V and a 820 ohm resistor on one end, and one of these lamp outputs on the other end.

Original PCB supplied by Antonio Nati
Reverse engineered by Matt Ownby with help from Warren Ondras
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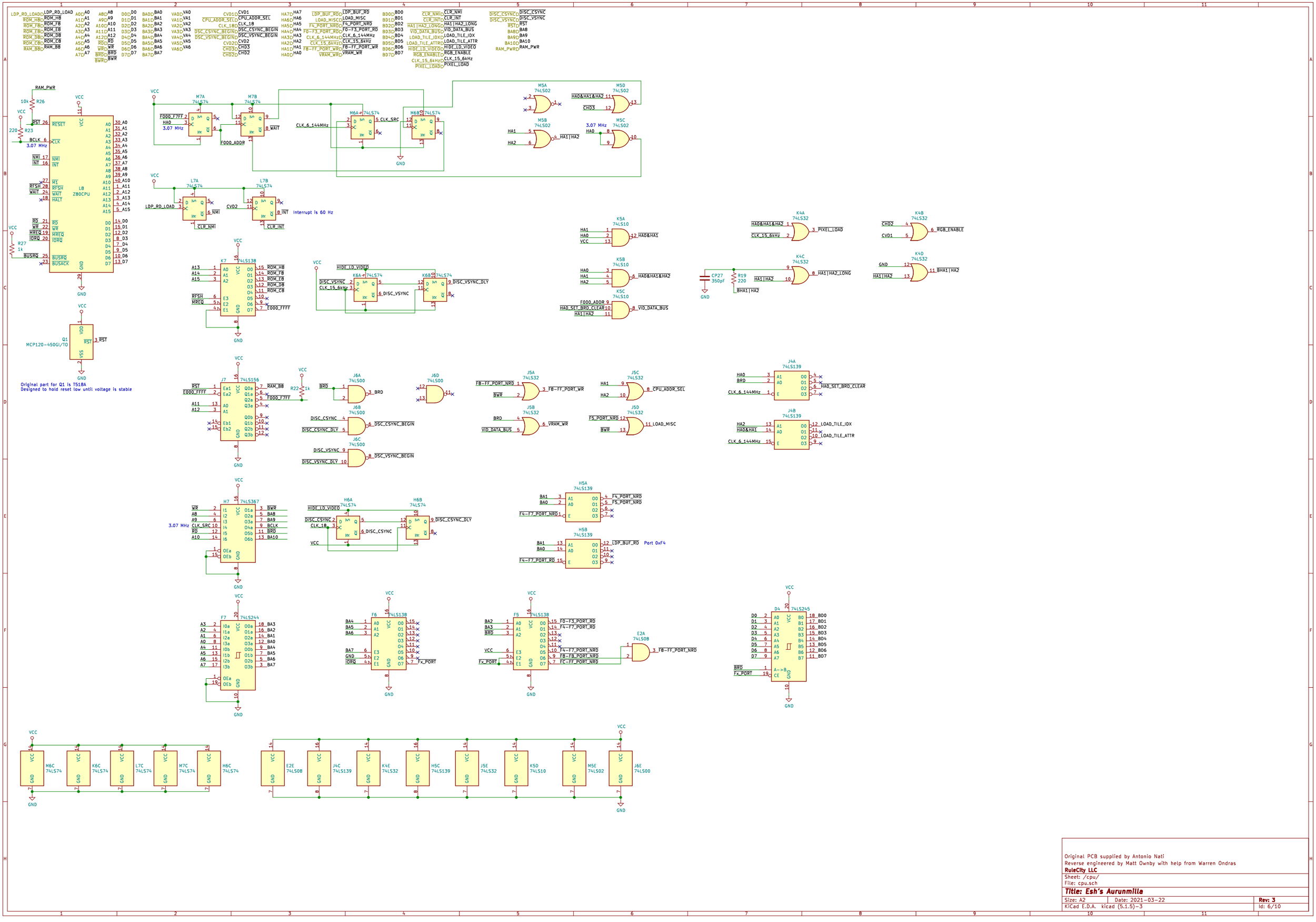
Sheet: /misc/
File: misc.sch

Title: Esh's Aurunmilla

Size: A4	Date: 2021-03-22	**Rev: 3**
KiCad E.D.A. kicad (5.1.5)-3		Id: 5/10



Original PCB supplied by Antonio Nati
Reverse engineered by Matt Ownby with help from Warren Ondras
RuleCity LLC

Sheet: /cpu/
File: cpu.sch

Title: Esh's Aurunmilla

Size: A2	Date: 2021-03-22	**Rev: 3**
KiCad E.D.A. kicad (5.1.5)-3		Id: 6/10

VRAM_WR
HA1|HA2_LONG
VID_DATA_BUS
BRD
CLK_7_8kHz
VA0
VA1
VA3
LOAD_TILE_IDX
LOAD_TILE_ATTR
D0 D1 D2 D3 D4 D5 D6 D7
MA0 MA1 MA2 MA3 MA4 MA5 MA6 MA7 MA8 MA9 MA10
IN0_RGB_A8 IN1_RGB_A8 IN2_RGB_A8 IN3_RGB_A8
HIDE_LD_VID_PAL1 HIDE_LD_VID_PAL0
HIDE_LD_VIDEO RGB_ENABLE PIXEL_LOAD CLK_6_144MHz
ANALOG_RED ANALOG_GREEN ANALOG_BLUE SHOW_LD_VIDEO

The fact that only the lowest 3 vertical address bits change per tile "proves" that tiles are 8 pixels high

M3 2732 — CLK_7_8kHz, VA0, VA1, VROM_A3, VROM_A4, VROM_A5, VROM_A6, VROM_A7, VROM_A8, VROM_A9, VROM_A10, B2D4 → M3_D0..M3_D7 — aka "A"
L3 2732 — same address lines → L3_D0..L3_D7 — aka "B"
K3 2732 — same address lines → K3_D0..K3_D7 — aka "C"

Pixel Shifters

The fact that 8 bits are shifted in per pixel load "proves" that each tile is 8 pixels wide

M1 74LS166: M3_D0..M3_D7 → RGB_A0
L1 74LS166: L3_D0..L3_D7 → RGB_A1
K1 74LS166: K3_D0..K3_D7 → RGB_A2
PE ← PIXEL_LOAD; Clk ← CLK_6_144MHz; CE, Clr

H4 holds tile attribute.
Lower nibble holds color palette.
Bit 6–7 determines which MISC value is used to modify color palette
(this is used to make the tile blink; different values determine blink frequency
or whether blinking is disabled)

H4 74LS174: B2D7, B2D1, B2D6, B2D3, B2D2, B2D0 → PALETTE_MOD_SEL1, RGB_A4, PALETTE_MOD_SEL0, RGB_A6, RGB_A5, RGB_A3; Cp ← LOAD_TILE_ATTR

H3 holds tile index.

H3 74LS273: B2D5, B2D6, B2D1, B2D7, B2D0, B2D2, B2D3, B2D4 → VROM_A8, VROM_A9, VROM_A4, VROM_A10, VROM_A3, VROM_A5, VROM_A6, VROM_A7; Cp ← LOAD_TILE_IDX

H2 74LS153: HIDE_LD_VID_PAL1 selects; IN0_RGB_A8..IN3_RGB_A8 → RGB_A7, RGB_A8; PALETTE_MOD_SEL0, PALETTE_MOD_SEL1

J1 MB7124: RGB_A8..RGB_A3 → RGB_D7..RGB_D3; CE ← RGB_ENABLE; RGB_A2..RGB_A0 → RGB_D2..RGB_D0; R16 1k

Digital->Analog conversion

RGB_D0 — R9 1k
RGB_D1 — R8 470
RGB_D2 — R7 220 → ANALOG_RED
RGB_D6 — R6 220
RGB_D5 — R5 470 → ANALOG_BLUE
RGB_D4 — R4 470
RGB_D3 — R3 220 → ANALOG_GREEN

F4 74LS245: D0..D7 → B2D0..B2D7; BRD, VID_DATA_BUS → A->B, CE

F3 M58725 — Generic 6116 RAM should serve as a replacement for this video RAM.
MA10 MA9 MA8 MA7 MA6 MA5 MA4 MA3 MA2 MA1 MA0 → B2D0..B2D7; WE ← VRAM_WR; CS ← E2D 74LS08 (VID_DATA_BUS, HA1|HA2_LONG)

F2C 74LS02: HIDE_LD_VID_PAL0, HIDE_LD_VID_PAL1 → HIDE_LD_VIDEO
F2B 74LS02: HIDE_LD_VIDEO → HIDE_LD_VIDEO
E2C 74LS08: HIDE_LD_VIDEO, RGB_D7 → SHOW_LD_VIDEO

RGB_D7 high means color is transparent. Otherwise, opaque.

Original PCB supplied by Antonio Nati
Reverse engineered by Matt Ownby with help from Warren Ondras
RuleCity LLC

Sheet: /video/
File: video.sch

Title: Esh's Aurunmilla

Size: A3 | Date: 2021-03-22 | **Rev: 3**
KiCad E.D.A. kicad (5.1.5)-3 | Id: 7/10

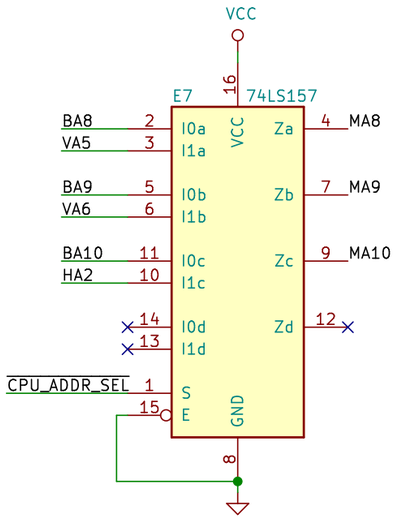
MA0 MA1 MA2 MA3 MA4 MA5 MA6 MA7 MA8 MA9 MA10

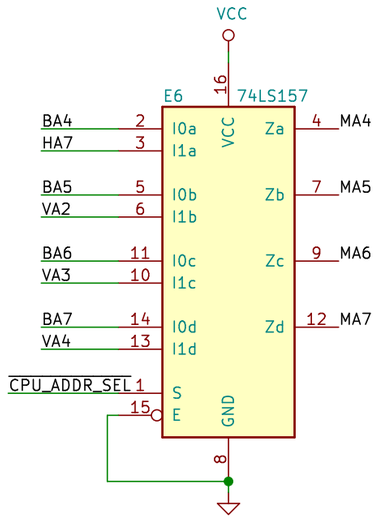
BA0 BA1 BA2 BA3 BA4 BA5 BA6 BA7 BA8 BA9 BA10

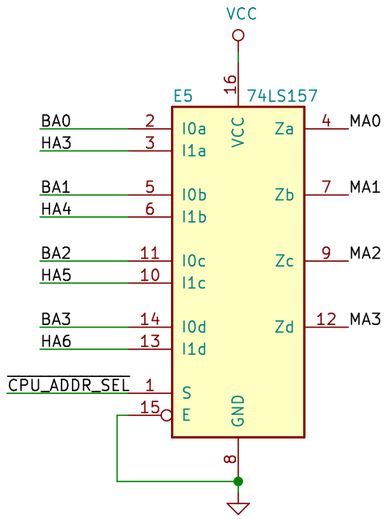
VA2 VA3 VA4 VA5 VA6 HA2 HA3 HA4 HA5 HA6 HA7

CPU_ADDR_SEL

So CPU can modify video RAM, while also allowing computer-generated video to be constantly redrawn







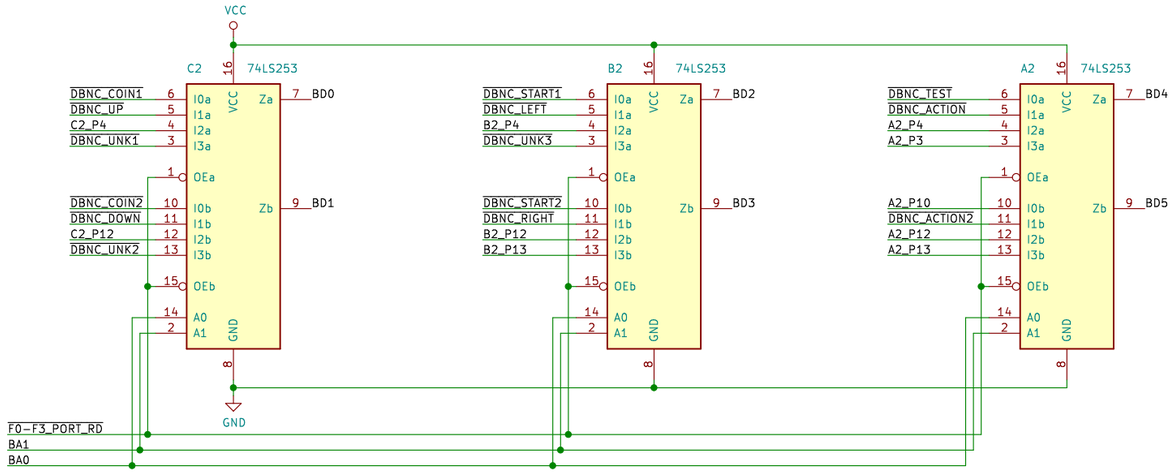
Original PCB supplied by Antonio Nati
Reverse engineered by Matt Ownby with help from Warren Ondras
RuleCity LLC

Sheet: /addrmux/
File: addrmux.sch

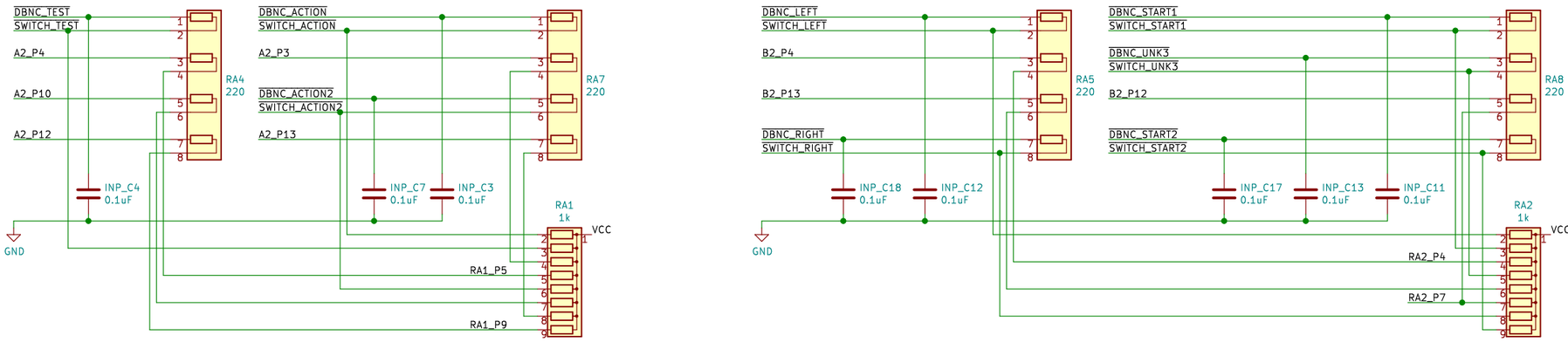
Title: Esh's Aurunmilla

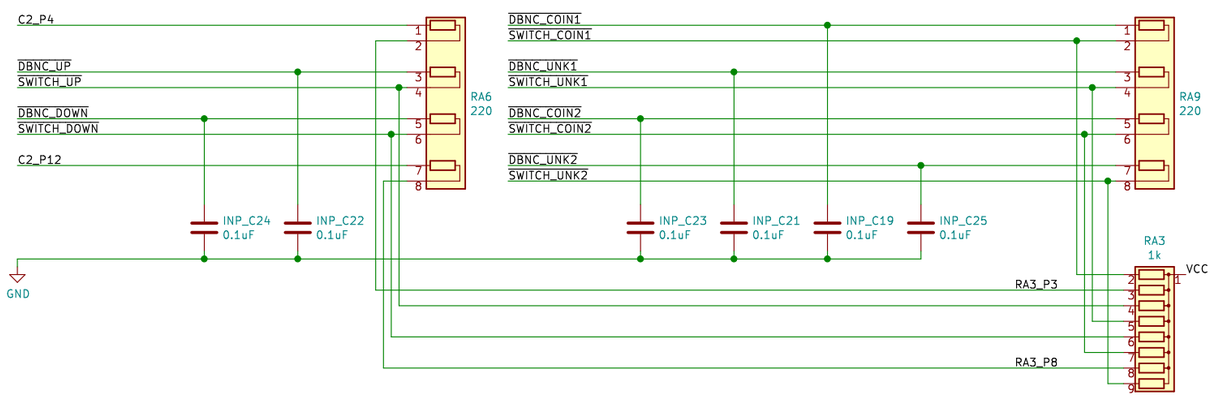
Size: A4	Date: 2021-03-22	**Rev: 3**
KiCad E.D.A. kicad (5.1.5)-3		Id: 8/10

F0-F3_PORT_RD
BA1
BA0
BD0
BD1
BD2
BD3
BD4
BD5
SWITCH_TEST
SWITCH_ACTION
SWITCH_ACTION2
SWITCH_LEFT
SWITCH_RIGHT
SWITCH_START1
SWITCH_UNK3
SWITCH_START2
SWITCH_COIN1
SWITCH_UNK1
SWITCH_COIN2
SWITCH_UNK2
SWITCH_UP
SWITCH_DOWN
RA2_P7
RA2_P4
RA3_P3
RA3_P8
RA1_P5
RA1_P9



Unused inputs are connected to pull-ups as a precaution



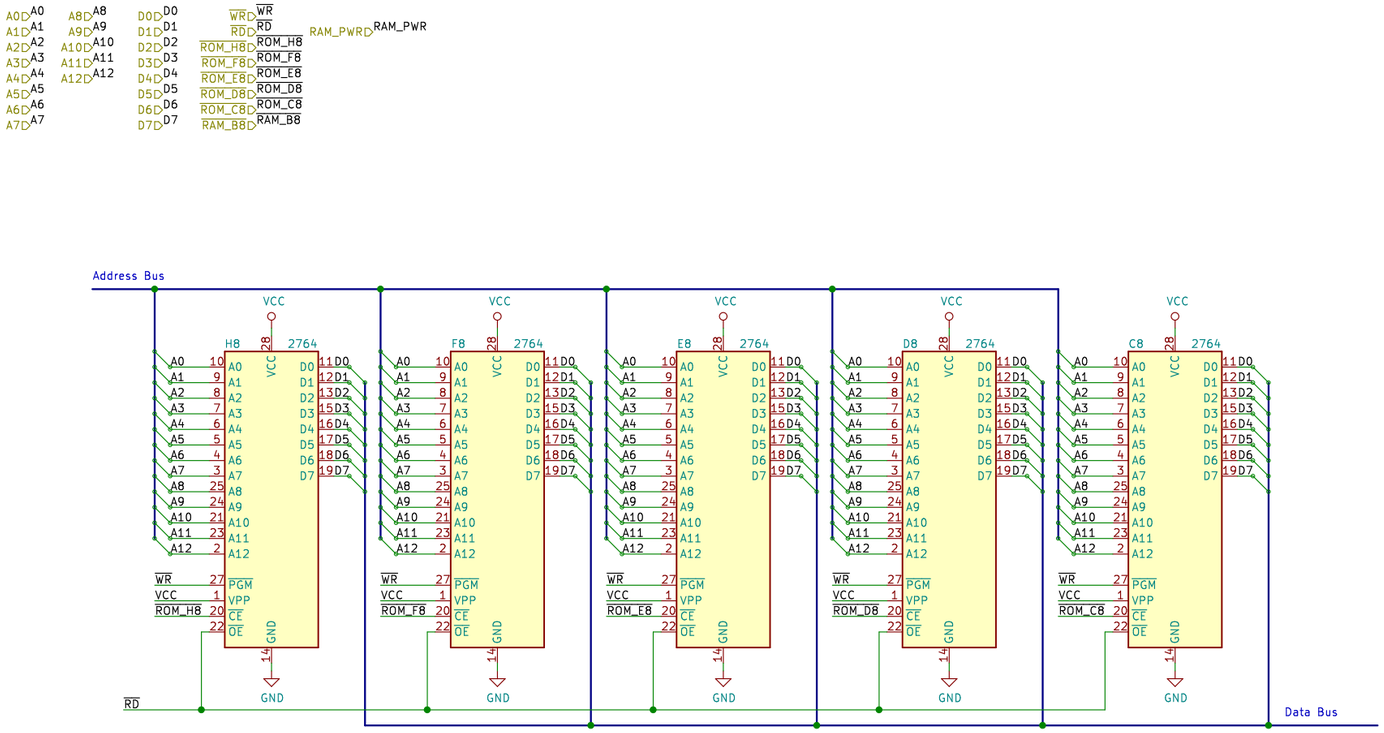


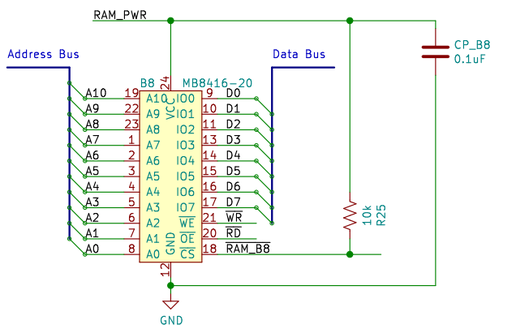
Original PCB supplied by Antonio Nati
Reverse engineered by Matt Ownby with help from Warren Ondras
RuleCity LLC

Sheet: /input/
File: input.sch

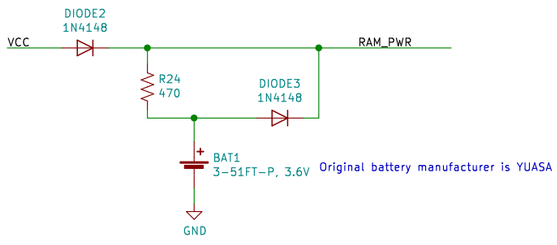
Title: Esh's Aurunmilla

Size: A3	Date: 2021-03-22	**Rev: 3**
KiCad E.D.A. kicad (5.1.5)-3		Id: 9/10





This is the CPU's RAM. Generic 6116 RAM should work as a replacement.



When powered on, RAM_PWR is VCC - 0.6V
(measured VCC at 4.8V, RAM_PWR at 4.2V)
When powered off, RAM_PWR is the battery's voltage

Original PCB supplied by Antonio Nati
Reverse engineered by Matt Ownby with help from Warren Ondras
RuleCity LLC

Sheet: /memory/
File: memory.sch

Title: Esh's Aurunmilla

Size: A3	Date: 2021-03-22	**Rev: 3**
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